

LIN Bus Shunt Slave Node Position Detection

Revision 1.0

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REVISION HISTORY

| Issue | Date | Remark |
|--------------|------------|-------------------------|
| Revision 1.0 | 2008-12-10 | 1 st release |
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1 SCOPE

This document is intended to describe a method for the detection of the position of a particular slave node in a LIN network with equal built slaves. This does not limit the use of position detection to the method described here.

The document covers the Bus Shunt Method

1.1 REFERENCES

- [1] LIN Specification Package, Revision 2.1, 2006-11-24
- [2] Electromagnetic compatibility (EMC)- Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test, IEC 61000-4-2: 1995



2 **REQUIREMENTS**

The specified methods must provide a means to assign a slave node with a unique node address within the particular LIN network, which can be used to configure the nodes according to LIN 2.1.

Any Slave Node Position Detection method should not violate the LIN Specification. In case an SNPD method violates the LIN Specification, these violations are described in the following chapters with the respective method descriptions. The behavior is described in the chapter "Limitations in Use" of the respective method description.



3 BUS SHUNT METHOD (BSM)

3.1 CONTENTS OF THIS CHAPTER

This chapter gives a guideline for the design of a LIN system with standard slaves and slaves capable of node position detection via the Bus Shunt Method by only looking into the rules for the Bus Shunt Method (BSM) part of the system.

3.2 BUS ARCHITECTURE

The following diagram shows a bus architecture using the Bus Shunt Method (BSM).



Figure 3-1: Typical bus architecture

On the left side of the schematic the master node is terminating the LIN bus. Next to it is a standard LIN node followed by a BSM slave node and so on. The BSM slave nodes and standard LIN nodes may be arranged in any order. The start of the addressing sequence is initialized by the master node, with a command sent to the slaves telling them that the addressing sequence starts with the next break. During the next break each slave starts its own sequence. The sequence is divided up in switching the slave pull-up resistor and current sources on and off, measuring the offset current, making a pre-selection, and then at the end, selection of the last not addressed BSM slave node in the line. Each slave stores its new NAD and is now addressable over this new NAD. If all slaves have received their new NAD, the master can now program this information into the SNPD node with a separate programming command if NVM is available.



3.3 PRINCIPLE

The Bus Shunt Method (BSM) works as follows:

During a break the current on the LIN Bus depends on the position on the bus. The BSM is routing the LIN Bus through a shunt on the SNPD node in order to be able to measure the current of the LIN Bus. In order to have reproducible currents – independent of the supply voltage, the pull up resistors are switched off and current sources are switched on during this process in the following matter:

The break is divided into 7 steps, in which the current conditions on the bus change and the measurements take place:

- 1. During the first step all current sources and the pull up resistors of the involved SNPD nodes are switched off. This way only the pull up resistors of nodes not using the shunt method contributes to the current on the bus line.
- During the second step each SNPD node measures the current flowing through the shunt of the SNPD node. The measured current is called I_{shunt_1} and is the offset current on the bus line.
- 3. During the third step, a pre selection of the slaves is done, for this, current sources 1 in all SNPD nodes are switched on. All nodes that have been already identified in a previous cycle keep all their current sources and pull up resistors switched off.
- 4. During the fourth step, each SNPD node measures again the current on the LIN Bus flowing through the shunt of the SNPD node. The measured current is called I_{shunt_2}. The value of the difference between this current (I_{shunt_2}) and the offset current (I_{shunt_1}) indicates, whether it could be one of the most distant SNPD nodes from the master. If the difference is below a specific value I_{Diff} the SNPD node is being considered as one of the last SNPD nodes in line. These SNPD nodes are called "pre-selected" SNPD nodes.
- The next step is divided into two actions. First action (A), all not pre-selected SNPD nodes switch their current sources 1 off. Second action (B), all pre-selected SNPD nodes switch their current sources 2 on (The current sources 1 of the preselected SNPD nodes remain switched on. The pull up resistors of all SNPD nodes remain switched off.)
- 6. In the sixth step, the current through the SNPD node is measured again. The measured current is called I_{shunt_3}. If the difference between this current (I_{shunt_3}) and the offset current (I_{shunt_1}) is below a specific threshold value I_{Diff} the SNPD node is identified as the last not addressed SNPD node in the bus line. This SNPD node then stores the transmitted NAD in to its RAM and the master can now communicate with the SNPD node using this NAD.
- 7. During the seventh step, all current sources are switched off and all pull up resistors of the SNPD nodes are switched on, in order to resume to the normal bus mode.







3.4 PHYSICAL LAYER

3.4.1 Description of the needed components

The position detection feature added to the normal LIN bus functionality allows a slave to detect if it is the last one in line without an address. The additional hardware resources needed for that purpose are a shunt resistor between the BUS_IN and a new output pin BUS_OUT of the slave and a circuitry that allows measuring the current in the bus shunt resistor. For the injection of a constant current during positioning detection two controlled current sources and the possibility to switch off standard pull-up are required.

3.4.2 LIN transceiver for BSM-nodes (principle)

The LIN transceiver consists of a transmit and a receive signal path. The receiver path is represented by a comparator that is comparing the bus signal against a mean reference voltage. The output of this comparator is the internal signal RXD. The transmit path consists of a low side driver between the bus line and ground. For a dominant bus signal this driver has to be activated over the internal TXD signal. Between TXD and the driver transistor additional circuitry for slew rate control and current limitation has been implemented. In order to comply with negative bus voltages referred to the local ground potential, a diode has been inserted in series to the output driver. Additionally a bus pull-up resistor together with a series diode between the bus line and V_{Sup} belongs to the standard LIN transceiver. In a BSM node this pull-up path is enabled over the internal control_1 signal. For the position detection capability, two additional current sources and diodes are also included in to the LIN transceiver. These sources may be enabled over the control signal 1 & 2. Together with the bus shunt resistor R_{SHUNT} it is possible for a slave node to determine its position on the LIN bus.

Remark: In normal Mode, the parameters of the LIN 2.1 specification are recommended. In applications, with un-powered nodes it is useful to reduce the value $I_{BUS_no_bat}$ to 1µA, to reduce the quiescent current in the system (see LIN Physical Layer Spec. Rev. 2.1).

The following simplified schematic shows the BSM LIN bus transceiver circuitry:



Figure 3-3: Schematic of the BSM transceiver circuitry

3.4.3 Differential amplifier (principle)

The differential amplifier is sampling and amplifying the differential input voltage between BUS_IN and BUS_OUT. Between these two terminals the shunt resistor is measuring the bus current. The differential amplifier needs a low offset because of the low voltages across the shunt. If needed the gain of the amplifier could be temperature compensated, to compensate the temperature coefficient of the shunt resistor.

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|----------------------------|--|
| LOCAL INTERCONNECT NETWORK | , , , , |

3.4.4 Signal acquisition chain (principle)

The comparison between the different current levels can be made with sample and hold circuits and comparators or digitally with an ADC (Analogue to Digital Converter).

The following block diagram (Figure 3-4) shows the needed components for an ADC realization:



Figure 3-4: Components contributing to the signal path using an A/D converter

The voltage over the shunt resistor is measured via a differential amplifier. In addition to the output signal of the differential amplifier the ADC maybe used for any additional auxiliary signals on the chip. The reference voltage of the ADC can be a band gap reference trimmed to the desired precision. If an SC-Amplifier (Switched Capacitor Amplifier) is used, the conversion process has to be synchronized to the clock signal. This synchronization can be done automatically by a conversion control block as soon as the differential amplifier is selected as input source.

3.4.5 Pull-up current sources 1 & 2

The pull-up current sources are intended to generate a predefined pull-up current on the bus line. For normal bus operation the pull-up current sources are not needed and therefore they are disabled.



3.4.6 Timing Parameter

| no. | symbol | parameter | condition | min. | typ. | max. | unit |
|-----|-----------------------|--|--|------|------|------|-------|
| 1 | t _{on_CS_1} | Switching on time of current source 1 | Bus load conditions $C_{BUS} = 10nF$ $R_{BUS} = 500 \Omega$ | | | 5 | μs |
| 2 | t _{off_CS_1} | Switching off time of current source 1 | Bus load conditions $C_{BUS} = 10nF$ $R_{BUS} = 500 \Omega$ | | | 1 | μs |
| 3 | t _{on_CS_2} | Switching on time of current source 2 | Bus load conditions $C_{BUS} = 10$ nF $R_{BUS} = 500 \Omega$ | | | 5 | μs |
| 4 | t _{off_CS_2} | Switching off time of current source 2 | Bus load conditions $C_{BUS} = 10$ nF $R_{BUS} = 500 \Omega$ | | | 1 | μs |
| 5 | t _{on_Rpu} | Switching on time of the pull-up resistor | Bus load conditions $C_{BUS} = 10nF$ $R_{BUS} = 500 \Omega$ | | | 5 | μs |
| 6 | t _{off_Rpu} | Switching off time of the pull-up resistor | Bus load conditions $C_{BUS} = 10nF$ $R_{BUS} = 500 \Omega$ | | | 1 | μs |
| 7 | t_ _{MADC} | Measurement time ADC | The average value of at least 3 measurements are recom- mended | | | 120 | μs |
| 8 | T_MDAC_PD | Delay before the ADC measurement starts | | 10 | | | μs |
| 9 | t_ _{PD} | Propagation delay of detect- ing the break and starting the action | Including the Propagation de- lay of the transceiver | | | 5 | μs |
| 10 | t_mid | Timing definition of Step 5 first action (A) and second action (B) | Time from begin of Step 5 first action (A) to begin of second action (B). (See Figure 3-5) | 0,45 | 0,5 | 0,55 | T-Bit |

Table 3-1: Timing table

3.4.7 DC characteristics

| no. | symbol | parameter | condition | min. | typ. | max. | unit |
|-----|---------------------|--|-----------|------|------|------|------|
| 1 | I _{CS 1} | Pull-up current source_1 | 2) | 1 | | 1,24 | mA |
| 2 | I_ _{CS_2} | Pull-up current source_2 | 2) | 3,15 | | 3,85 | mA |
| 3 | R_{shunt} | Bus shunt resistor in the slave | 1) | 0,65 | | 1,25 | Ω |
| 4 | I _{Diff} | Selection and Pre- selection | | 2,3 | | 2,9 | mA |
| 5 | R_ _{Slave} | pull-up resistor in a slave | | 20 | | 60 | KΩ |
| 6 | R_Master | pull-up resistor in the master | | 900 | | 1100 | Ω |
| 7 | I_Bus_dom | Driving current in domi- nant state | 2) | 40 | | | mA |

Table 3-2: DC Characteristics

1) This resistor could also be located externally

2) The transceiver in the master ECU must be capable to drive at least 40mA for 9 T-Bit after 4 T-Bit of the falling edge of the break field.



3.4.8 Timing of the measurement sequence

In order to receive a correct behavior of the complete system, all SNPD nodes using the Bus Shunt Method have to use the same timing. The timing of the different steps is defined in the following table. The oscillator of the slave has to fulfill the same accuracy as for a slave to slave communication defined in the LIN specification.

| Step | Action | Start of action [T _{BIT}] |
|------|---|-------------------------------------|
| 1 | Switching off all Pull- Ups and all current sources | 1 (Falling edge of break field) |
| 2 | Start offset measurement (I_shunt_1) | 2 |
| 3 | Switching on current source 1 | 5 |
| 4 | Start the measurement 1 (I_shunt_2) | 6 |
| 5 | All not pre-selected (first action A) nodes switching off there current source_1 with the falling edge of the T_{BIT} signal. | 9 |
| | All pre selected SNPD (second action B) nodes are switching on their current source 2 with the rising edge of the T_{BIT} signal. | |
| 6 | Start the measurement 2 (I_shunt_3) | 10 |
| 7 | Switching off all current sources and switching on the pull-up | 14 |

Table 3-3: Timing of Bus Shunt Method Slave Node Position Detection

3.4.9 Timing in the SNPD node

To secure the sequence, in each BSM slave node the same sequence has to start.





3.4.10 Timing including tolerances

As defined in the LIN specification [1], section 6.3, a tolerance of the oscillator frequency from slave to slave is allowed. Therefore, a certain safety margin has to be taken into account when calculating the timing of the different steps.



Figure 3-6: Timing diagram including tolerances

3.5 SUB FUNCTIONS

The SNPD sub function IDs for the Bus Shunt method are summarized in the table below.

| SNPD sub function | Description | SNPD Sub function ID | | | | |
|---|---|----------------------|--|--|--|--|
| BSM Initialization | All BSM-nodes enter the un- configured mode | 0x01 | | | | |
| Next NAD | Informing all slaves about the next NAD | 0x02 | | | | |
| Store NAD | Store the assigned NADs in to the NVM of the slaves, if avail- able | 0x03 | | | | |
| BSM finished Informing all slaves that the procedure is finished 0x04 | | | | | | |
| Table 3-4: SNPD Sub Function IDs of the Bus Shunt Method | | | | | | |



<u>Note</u>

With the Bus Shunt Method, the implementation of SNPD sub functions 0x01, 0x02 and 0x04 is mandatory. There is no SNPD response to the BSM sub functions, only addressed slaves response to a request.

3.6 CONFIGURATION FLOW

Beginning with the BSM- Initialization, all SNPD nodes with BSM capability start their measurement sequence within the next break field.

Beginning with the "BSM initialization"-request SNPD sub function 0x01, all nodes capable of using the Bus Shunt Method are going into their "BSM- Mode" and start with each break field the BSM sequence. Within the command "Next NAD" sub function 0x02 all BSM slaves will be informed about the next NAD. The SNPD node which was the last not addressed node in the line, takes the NAD in to his RAM and this node can now response to this NAD. The Master sends now the "Next NAD" sub function 0x02 with the next NAD information and so on. With the command "Store NAD" sub function 0x03, all slaves with available NVM, store the NAD information in their NV-Memory. With the command "BSM Finished" sub function 0x04, all slaves stop their BSM sequence and they will not react to the 0x02, 0x03 and 0x04 sub function anymore, until the command "BSM initialization" sub function 0x01 is broad-casted again. Each node that has been configured (got a NAD) remains passive during the remaining BSM sequence. With this method the SNPD nodes are successively configured from the first SNPD node to the last SNPD node (closest to the master). While the addressing is ongoing, the master can optionally send other LIN commands, but only those BSM sequences with the PDU content is equal to the command "Next NAD" are valid.









3.6.3 BSM Setup Flow in Detail

| | | As | sign NAD | via SNPE | Request | | | | |
|-----------------------------------|-------------------------------|-------------------------|-----------------------|-----------------------|---------------------|----------------------|------------------------|--------------------|--------------------------|
| | | NAD | PCI | SID | D1 | D2 | D3 | D4 | D5 |
| Header 0x3C | + | Initial NAD | | | Supplier ID LSB | Supplier ID MSB | Function ID LSB | Function ID MSB | unused |
| | | 0x7f | 0x06 | 0xb5 | Oxff | 0x7f | 0x01 | 0x02 | Oxff |
| All SNPD slave ield | es with BSM | capability | y start th | neir mea | suremer | nt sequei | nce with | the next | break |
| | Oţ | otional: c | other (s | tandard | I) LIN Me | essages | | | |
| Assign NAD t | o slave 1 | | | | | | | | |
| | | As | sign NAD | via SNPE | Request | | | | |
| | | NAD | PCI | SID | D1 | D2 | D3 | D4 | D5 |
| Header | + | Initial NAD | | | Supplier ID LSB | Supplier ID MSB | Function ID LSB | Function ID MSB | New NAD |
| 0,00 | | 0x7f | 0x06 | 0xb5 | Oxff | 0x7f | 0x02 | 0x02 | New NAD fo Slave_2 |
| Il SNPD slave eld; after the l | es with BSM break field th | capability e selecte | y start th ed SNPE | neir mea D slave t | suremer akes the | nt sequer NAD for | nce withi r slave 1 | n the bre | eak |
| | Or | otional: c | other (s | tandard | I) LIN Me | essages | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | Website : v | ww.lin-s | ubbus.o | ora Cont | act: info | @lin-sub | bus.ora | | |



| Header 0x3C + NAD Initial NAD PCI Initial Initial Supplier IDLSB | | | Assię | gn NAD v | IA SNPD | Request | 1 | | T | 1 | | |
|--|--|--|---|--|-----------------------------------|--|---|--|--|--------------------------------------|--|--|
| Header 0x3C + Initial NAD Supplier 0x7f Supplier 0x06 Supplier 0x55 Supplier 0x8F Function 0x8F Net 0x8F All SNPD slaves with BSM capability start their measurement sequence within the break field; after the break field the selected SNPD slave takes the NAD for slave n Net site Optional: other (standard) LIN Messages Assign NAD to slave n+1 Assign NAD to slave n+1 Assign NAD to slave n+1 Header 0x3C Assign NAD to slave n+1 Assign NAD via SNPD Request Header 0x3C Assign NAD via SNPD slave swith BSM capability start their measurement sequence within the break field the selected SNPD slave takes the NAD for slave n+1 Optional: other (standard) LIN Messages Store NAD in slave (Optional) Assign NAD via SNPD Request Header 0x3C Assign NAD via SNPD Request MAD PCI SID D1 D2 D3 D4 1 MAD PCI SID D1 D2 D3 D4 1 ID MSB ID MSB ID MSB ID MSB ID LSB ID MSB | | | NAD | PCI | SID | D1 | D2 | D3 | D4 | D5 | | |
| Ox7f Ox06 Ox55 Oxff Ox7f Ox02 Nev All SNPD slaves with BSM capability start their measurement sequence within the break field; after the break field the selected SNPD slave takes the NAD for slave n Optional: other (standard) LIN Messages Optional: other (standard) LIN Messages Assign NAD to slave n+1 Assign NAD to slave n+1 Header Ox7f Ox06 Oxb5 Oxff Ox7f Ox02 Ox02 Nev MAD PCI SID D1 D2 D3 D4 II Header + Initial ID LSB ID MSB Function Function Nev Ox3C + 0x7f 0x06 0xb5 0xff 0x7f 0x02 0x02 Nev All SNPD slaves with BSM capability start their measurement sequence within the break field; after the break field the selected SNPD slave takes the NAD for slave n+1 Store NAD in slave (Optional) Assign NAD via SNPD Request Assign NAD via SNPD Request MAD PCI SID D1 D2 D3 D4 I | eader | + | Initial NAD | | | Supplier ID LSB | Supplier ID MSB | Function ID LSB | Function ID MSB | New NAD | | |
| All SNPD slaves with BSM capability start their measurement sequence within the break field the selected SNPD slave takes the NAD for slave n Optional: other (standard) LIN Messages Optional: other (standard) LIN Messages Assign NAD to slave n+1 Assign NAD to slave n+1 Header Ox3C NAD Assign NAD via SNPD Request Header Ox7f 0x06 0xb5 0xff 0x7f 0x02 0x02 Nev All SNPD slaves with BSM capability start their measurement sequence within the break field; after the break field the selected SNPD slave takes the NAD for slave n+1 Optional: other (standard) LIN Messages | | | 0x7f | 0x06 | 0xb5 | Oxff | 0x7f | 0x02 | 0x02 | New NAD for Slave_n | | |
| Optional: other (standard) LIN Messages Assign NAD to slave n+1 Assign NAD to slave n+1 Header NAD PCI SID D1 D2 D3 D4 IC NAD PCI SID D1 D2 D3 D4 IC Header + Initial NAD Supplier Supplier Function Function New Store All SNPD slaves with BSM capability start their measurement sequence within the break field; after the break field the selected SNPD slave takes the NAD for slave n+1 Optional: other (standard) LIN Messages Store NAD in slave (Optional) Assign NAD via SNPD Request Header 0x3C + NAD PCI SID D1 D2 D3 D4 I Header 0x3C + NAD PCI SID D1 D2 D3 D4 I Header 0x3C + NAD PCI SID D1 D2 D3 D4 I Header 0x3C + NAD PCI SID D1 D2 D3 D4 I < | SNPD slaves ld; after the bro | with BSM ca eak field the s | pability selected | start the SNPD | eir meas slave ta | urement kes the | t sequer NAD for | ice withi slave n | n the bre | eak | | |
| Optional: other (standard) LIN Messages Assign NAD to slave n+1 Assign NAD via SNPD Request + NAD PCI SID D1 D2 D3 D4 I Header 0x3C + NAD PCI SID D1 D2 D3 D4 I Header 0x3C + NAD PCI SID D1 D2 D3 D4 I Header 0x3C Ox7f 0x06 Oxbox SNPD Request Header 0x3C NAD PCI SID D1 D2 D3 D4 I Header 0x3C NAD PCI SID D1 D2 D3 D4 I Header 0x3C NAD <th <="" colspan="2" td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></th> | <td></td> | | | | | | | | | | | |
| Assign NAD to slave n+1 Assign NAD via SNPD Request Header 0x3C + NAD PCI SID N NAD N CO D <th colspan<="" td=""><td></td><td>Opti</td><td>onal: ot</td><td>her (sta</td><td>andard)</td><td>LIN Me</td><td>ssages</td><td></td><td></td><td></td></th> | <td></td> <td>Opti</td> <td>onal: ot</td> <td>her (sta</td> <td>andard)</td> <td>LIN Me</td> <td>ssages</td> <td></td> <td></td> <td></td> | | Opti | onal: ot | her (sta | andard) | LIN Me | ssages | | | | |
| Assign NAD to slave n+1 Assign NAD via SNPD Request Header 0x3C + $NAD \ PCl \ SID \ D1 \ D2 \ D3 \ D4 \ ID \ Supplier \ Supplier \ Supplier \ Supplier \ Supplier \ Supplier \ Function \ Function \ New \ ID \ NSB \ ID \ LSB \ ID \ NSB \ ID \ LSB \ ID \ NSB \ ID \ LSB \ ID \ MSB \ ID \ LSB \ ID \ MSB \ ID \ Supplier $ | | | | | | | | | | | | |
| Assign NAD to slave n+1 Assign NAD via SNPD Request Header 0x3C + NAD PCI SID D1 D2 D3 D4 I Header 0x3C + Initial NAD Supplier 0x7f Supplier 1D LSB Supplier 1D LSB Function 1D LSB New 1D LSB New 1SB New New Slav All SNPD slaves with BSM capability start their measurement sequence within the break ield; after the break field the selected SNPD slave takes the NAD for slave n+1 New NAD for slave n+1 New NAD for slave n+1 Store NAD in slave (Optional) Assign NAD via SNPD Request Header 0x3C + NAD PCI SID D1 D2 D3 D4 I NAD NAD PCI SID D1 D2 D3 D4 I NAD ISNPD slaves with BSM capability store their new NAD from the RAM in to the NVM, i available. | | | | | | | | | | | | |
| Assign NAD to SNPD Request Assign NAD via SNPD Request Header 0x3C + NAD PCI SID D1 D2 D3 D4 I Header 0x3C + NAD PCI SID D1 D2 D3 D4 I Header 0x3C Optional: other (standard) LIN Messages Store NAD in slave (Optional) Assign NAD via SNPD Request Header 0x3C + NAD PCI SID D1 D2 D3 D4 I Header 0x3C + NAD PCI SID D1 D2 D3 D4 I Header Ox7f Ox06 Ox05 Oxff DX7f DX03 D4 I I <td>sign NAD to</td> <td>slavo n±1</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> | sign NAD to | slavo n±1 | | | | | | | | | | |
| Header 0x3C+ $\begin{array}{ c c c c c c c c c c c c c c c c c c c$ | | | Accir | י חאא מי | | Request | | | | | | |
| Header 0x3C+INADPCISIDD1D2D3D4IInitial NADInitial NADSupplier ID LSBSupplier ID LSBFunction ID LSBFunction ID MSBNev ID LSBAll SNPD slaves with BSM capability start their measurement sequence within the break ield; after the break field the selected SNPD slave takes the NAD for slave n+1Optional: other (standard) LIN MessagesStore NAD in slave (Optional)Assign NAD via SNPD RequestHeader 0x3C+ $\frac{NAD}{PCI}$ SIDD1D2D3D4IHeader 0x3C+ $\frac{NAD}{PCI}$ SIDD1D2D3D4IHeader 0x3C-+ $\frac{NAD}{PCI}$ SIDD1 </td <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>D2</td> <td>20</td> <td></td> <td>Df</td> | | | | | | | D 2 | 20 | | Df | | |
| Header 0x3C + Initial NAD Supplier ID LSB Supplier ID LSB Supplier ID LSB Function ID LSB Function ID LSB Function ID LSB Nev ID LSB All SNPD slaves with BSM capability start their measurement sequence within the break field; after the break field the selected SNPD slave takes the NAD for slave n+1 Optional: other (standard) LIN Messages Store NAD in slave (Optional) Assign NAD via SNPD Request Header 0x3C + NAD PCI SID D1 D2 D3 D4 I Header 0x3C + NAD PCI SID D1 D2 D3 D4 I Header 0x3C - - Supplier Supplier Supplier Function Function Initial NAD PCI SID D1 D2 D3 D4 I Header 0x3C - - Supplier Supplier Function Function In All SNPD slaves with BSM capability store their new NAD from the RAM in to the NVM, i available. - - - - | | | | | 50 | | DZ Supelier | U3 | U4 | | | |
| UX3C 0x7f 0x06 0xb5 0xff 0x7f 0x02 0x02 Nev Stav All SNPD slaves with BSM capability start their measurement sequence within the break ield; after the break field the selected SNPD slave takes the NAD for slave n+1 Optional: other (standard) LIN Messages Optional: other (standard) LIN Messages Store NAD in slave (Optional) Assign NAD via SNPD Request Header 0x3C + NAD PCI SID D1 D2 D3 D4 I Initial NAD ID LSB ID MSB ID LSB ID MSB ID | eader | + | Initial NAD | | | Supplier ID LSB | Supplier ID MSB | Function ID LSB | Function | New NAD | | |
| All SNPD slaves with BSM capability start their measurement sequence within the break ield; after the break field the selected SNPD slave takes the NAD for slave n+1 Optional: other (standard) LIN Messages Store NAD in slave (Optional) Assign NAD via SNPD Request Header 0x3C + <u>NAD PCI SID D1 D2 D3 D4 I</u> Initial NAD ID LSB ID MSB ID MSB ID LSB ID MSB | x3C | | 0x7f | 0x06 | 0xb5 | 0xff | 0x7f | 0x02 | 0x02 | New NAD | | |
| All SNPD slaves with BSM capability start their measurement sequence within the break ield; after the break field the selected SNPD slave takes the NAD for slave n+1 Optional: other (standard) LIN Messages Store NAD in slave (Optional) Assign NAD via SNPD Request Header 0x3C + NAD PCI SID D1 D2 D3 D4 I Initial Supplier Supplier Function Function ID LSB ID MSB ID LSB ID MSB ID LSB ID MSB | | | | | | | | | | Slave_n+ | | |
| ield; after the break field the selected SNPD slave takes the NAD for slave n+1 Optional: other (standard) LIN Messages Store NAD in slave (Optional) Assign NAD via SNPD Request Header 0x3C NAD PCI SID D1 D2 D3 D4 I Initial NAD Supplier ID LSB Supplier ID LSB Function ID LSB Initial ID MSB Supplier ID LSB Supplier ID MSB Function ID MSB Initial ID MSB Initial I | | | | | | | | | | | | |
| Optional: other (standard) LIN Messages Store NAD in slave (Optional) Assign NAD via SNPD Request Header NAD PCI SID D1 D2 D3 D4 I Initial NAD ID LSB Supplier Function Function un 0x3C + Initial Supplier Supplier Function ID MSB ID IS ID < | SNPD slaves | with BSM ca | pability : | start the | ir meas | urement | t sequer | ice withi | n the bre | eak | | |
| Optional: other (standard) LIN Messages Store NAD in slave (Optional) Assign NAD via SNPD Request Header 0x3C NAD PCI SID D1 D2 D3 D4 I Header 0x3C NAD PCI SID D1 D2 D3 D4 I Header 0x3C O1 D2 D3 D4 I Header 0x3C + Initial NAD ID LSB < | SNPD slaves | with BSM ca eak field the s | pability selected | start the SNPD | eir meas slave ta | urement kes the | t sequer NAD for | ice withi slave n· | n the bre +1 | eak | | |
| Optional: other (standard) LIN Messages Store NAD in slave (Optional) Assign NAD via SNPD Request Header NAD PCI SID D1 D2 D3 D4 I NAD Initial Supplier Supplier Function Function Initial ID LSB ID MSB ID MSD ID MSD <td>SNPD slaves ld; after the bro</td> <td>with BSM ca eak field the s</td> <td>pability selected</td> <td>start the SNPD</td> <td>eir meas slave ta</td> <td>urement kes the</td> <td>t sequer NAD for</td> <td>ice withi slave n·</td> <td>n the bre +1</td> <td>eak</td> | SNPD slaves ld; after the bro | with BSM ca eak field the s | pability selected | start the SNPD | eir meas slave ta | urement kes the | t sequer NAD for | ice withi slave n· | n the bre +1 | eak | | |
| Store NAD in slave (Optional) Assign NAD via SNPD Request Header NAD PCI SID D1 D2 D3 D4 I NAD Initial Supplier Supplier Supplier Function Iunitial Initial Initial Initial ID LSB ID LSB ID MSB ID LSB ID MSB MSB ID MSD | SNPD slaves ld; after the bro | with BSM ca eak field the s | L pability s selected | start the SNPD | ir meas slave ta | urement kes the | t sequer NAD for | ice withi slave n∙ | n the bro +1 | eak | | |
| Store NAD in slave (Optional) Assign NAD via SNPD Request Header NAD PCI SID D1 D2 D3 D4 I Initial Initial Supplier Supplier Function Function Iunder 0x3C Value 0x7f 0x06 0xb5 0xff 0x7f 0x03 0x02 0 All SNPD slaves with BSM capability store their new NAD from the RAM in to the NVM, in available. Supplier | SNPD slaves ld; after the bro | with BSM ca eak field the s Opti e | pability selected | start the SNPD | slave ta | LIN Me | NAD for | slave n | n the bre +1 | eak | | |
| Store NAD in slave (Optional) Assign NAD via SNPD Request Header NAD PCI SID D1 D2 D3 D4 I Initial Initial Supplier Supplier Function Function Iunitial Initial ID LSB ID LSB ID LSB ID MSB ID MSB ID MSB Initial Initial ID LSB ID LSB ID LSB ID MSB | SNPD slaves ld; after the bro | with BSM ca eak field the s Opti e | pability selected | start the SNPD | ir meas slave ta | Lin Me | t sequer NAD for ssages | ice withi slave n· | n the bre | eak | | |
| Store NAD in Slave (Optional) Assign NAD via SNPD Request Header NAD PCI SID D1 D2 D3 D4 I Initial Initial Supplier Supplier Function In In NAD Initial Initial Supplier Supplier Function In In NAD ID ID LSB ID LSB ID LSB ID LSB ID MSB MSB ID MSB ID MSB ID MSB MSD MSB ID MSB MSD MSD ID MSB MSD MSD ID MSD MSD <td>SNPD slaves ld; after the bro</td> <td>with BSM ca eak field the s Optio</td> <td>pability selected</td> <td>start the SNPD</td> <td>ir meas slave ta</td> <td>LIN Me</td> <td>t sequer NAD for ssages</td> <td>slave n</td> <td>n the bre</td> <td>eak</td> | SNPD slaves ld; after the bro | with BSM ca eak field the s Opti o | pability selected | start the SNPD | ir meas slave ta | LIN Me | t sequer NAD for ssages | slave n | n the bre | eak | | |
| NAD VIa SNPD Request Header + NAD PCI SID D1 D2 D3 D4 I Initial Initial Supplier Supplier Supplier Function In In NAD 0x7f 0x06 0xb5 0xff 0x7f 0x03 0x02 0 All SNPD slaves with BSM capability store their new NAD from the RAM in to the NVM, in available. In | SNPD slaves ld; after the br | with BSM ca eak field the s Optio | pability selected | start the SNPD | ir meas slave ta | LIN Me | sequer NAD for | slave n | n the bre | eak | | |
| Header 0x3C+NADPCISIDD1D2D3D4IInitial NADInitial NADSupplier ID LSBSupplier ID LSBFunction ID LSBFunction ID LSBFunction ID LSBImage: Supplier ID LSBFunction ID LSBImage: Supplier ID LSBAll SNPD slaves with BSM capability store their new NAD from the RAM in to the NVM, in available. | SNPD slaves ld; after the bro | with BSM ca eak field the s Optiona | pability selected | her (sta | ir meas slave ta | LIN Me | ssages | ice withi slave n· | n the bre | eak | | |
| Header 0x3C + Initial NAD Initial NAD Supplier ID LSB Supplier ID MSB Function ID LSB Function ID MSB III MSB 0x7f 0x06 0xb5 0xff 0x7f 0x03 0x02 0x02 All SNPD slaves with BSM capability store their new NAD from the RAM in to the NVM, in available. | SNPD slaves ld; after the bro | with BSM ca eak field the s Optiona | pability selected | start the SNPD | ir meas slave ta andard) | LIN Me | ssages | slave n | n the bre | eak | | |
| 0x7f 0x06 0xb5 0xff 0x7f 0x03 0x02 0 All SNPD slaves with BSM capability store their new NAD from the RAM in to the NVM, i available. | SNPD slaves ld; after the bri ore NAD in sl | with BSM ca eak field the s Optiona | pability selected | start the SNPD her (sta gn NAD v PCI | ia SNPD | LIN Me | ssages | bce within slave n- | n the bre +1 | eak | | |
| All SNPD slaves with BSM capability store their new NAD from the RAM in to the NVM, i available. | SNPD slaves ld; after the bro bre NAD in slaves eader x3C | with BSM ca eak field the s Optiona ave (Optiona | initial NAD | start the SNPD her (sta | ia SNPD | LIN Me Request D1 Supplier ID LSB | D2 Supplier ID MSB | D3 Function ID LSB | D4 | D5 unused | | |
| | SNPD slaves ld; after the bro ore NAD in slaves eader x3C | with BSM ca eak field the s Optiona ave (Optiona | il) Assig NAD Initial NAD Ox7f | start the SNPD her (sta pn NAD v PCI 0x06 | ia SNPD SID 0xb5 | LIN Me Request D1 Supplier ID LSB Oxff | D2 Supplier ID MSB 0x7f | D3 Function ID LSB 0x03 | D4 Function ID MSB 0x02 | D5 unused 0xff | | |
| | SNPD slaves ld; after the bro ore NAD in slaves eader x3C SNPD slaves ailable. | with BSM ca eak field the s Optiona ave (Optiona + | bability selected | gn NAD v PCI 0x06 store th | ia SNPD SID 0xb5 eir new | LIN Me Request D1 Supplier ID LSB Oxff NAD fro | D2 Supplier ID MSB 0x7f m the R | D3 Function ID LSB 0x03 AM in to | D4 Function ID MSB 0x02 the NV | D5 unused 0xff M, if | | |
| | SNPD slaves ld; after the bro bre NAD in slaves eader x3C SNPD slaves ailable. | with BSM ca eak field the s Optiona ave (Optiona + | pability selected | start the SNPD her (sta pn NAD v PCI 0x06 store th | ia SNPD SID 0xb5 eir new | LIN Me Request D1 Supplier ID LSB Oxff NAD fro | D2 Supplier ID MSB 0x7f m the R | D3 Function ID LSB 0x03 AM in to | D4 Function ID MSB 0x02 the NV | eak D5 unused Oxff M, if | | |

| | NETWORK | | | | | Slave Dece | LIN E Node F Rev ember 1 | Bus Shu Position /ision 1.(0, 2008 | nt Detection) ; Page 20 |
|-----------------|---------------|-----------------|-----------|----------|-----------|---------------|-----------------------------------|--|-----------------------------------|
| | Optic | onal: oth | ner (star | ndard) I | LIN Mes | sages | | | |
| | | | | | | | | | |
| Assign NAD Fi | nished | | | | | | | | |
| | | Assig | n NAD via | | | <u>D2</u> | 20 | | D5 |
| Header | + | Initial | | | Supplier | Supplier | Function | Function | unused |
| 0,30 | | 0x7f | 0x06 | 0xb5 | Oxff | 0x7f | 0x04 | 0x02 | Oxff |
| All SNPD slaves | s with BSM ca | L pability s | top their | · measu | irement : | sequen | l ce in the | e break f | ield |
| | Website : ww | w.lin-suk | obus.org | Contac | t: info@l | in-subb | us.org | | |



3.7 EXAMPLE OF SETUPS OF A LIN BUS SYSTEM WITH BSM

Remark:

1. The following calculations are done with corner values

2. The transceiver in the master has to allow 40mA for 9 T-Bit times after 4 T-Bit times after the falling edge of the break field.

3.7.1 Calculation of the pre selected slaves for step 5 + 6

To calculate the corner situation it is necessary that we use the maximal threshold level and the smallest current out of current source 1 for the pre-selection.

| | | | Pre se slaves | electe s | d |
|-------------------------|------------------|--------------------------------------|------------------|-------------|-----|
| Threshold value | Condition | Calculation | min | type | max |
| Diff2-1 | Current source 1 | of the number of pre selected slaves | | | |
| Min = $2,3 \text{ mA}$ | Min = 1000 µA | I _{Diff} | | | |
| Type = $2,6 \text{ mA}$ | Type = 1100 μA | | 1 | | 3 |
| Max = 2,9 mA | Max = 1240 µA | current of current source 1 | | | |

Table 3-5: Calculation of pre selected slaves

3.7.2 Reference calculation of a system with 15 Standard- slaves

| No. | Parameter | Condition V _{bat} = 18V | $R_{Master} = 900 \ \Omega$ | $R_{Master} = 1100 \ \Omega$ |
|-----|------------|--|-----------------------------|------------------------------|
| | | Standard Nodes = 15 R_Slave = 20 k Ω | 13,5 mA | 13,5 mA |
| 1 | | BSM- Nodes = 0 I_ _{CS_1} = 1,24 mA | 0 mA | 0 mA |
| | I_R_Master | | 20 mA | 16,4 mA |
| | I_Bus_DOM | Current in the mas- ter transceiver | 33,5 mA | 29,9 mA |

Table 3-6: Calculation of a system with 15 Standard- slaves



3.7.3 Calculation of a system with 15 BSM- slaves

| No. | Parameter | Condition V _{bat} = 18V | $R_{Master} = 900 \ \Omega$ | $R_{Master} = 1100 \ \Omega$ |
|-----|------------|---|-----------------------------|------------------------------|
| 1 | Step 3 + 4 | Standard Nodes = 0 R_Slave = 20 kΩ | 0 mA | 0 mA |
| | | BSM- Nodes = 15 I_ _{CS_1} = 1,24 mA | 18,6 mA | 18,6 mA |
| | _R_Master | | 20 mA | 16,4 mA |
| | I_Bus_DOM | Current in the mas- ter transceiver | 38,6 mA | 35,0 mA |

| 2 | Step 5 + 6 | Standard Nodes = 0 R_Slave = 20 k Ω | 0 mA | 0 mA |
|---|------------|--|----------|----------|
| | | I_ _{CS_1} = 1,24 mA BSM- nodes = 3 3,72 mA 1) | | 3,72 mA |
| | | I _{_CS_2} = 3,85mA BSM- nodes = 3 1) | 11,55 mA | 11,55 mA |
| | I_R_Master | | 20 mA | 16,4 mA |
| | I_Bus_DOM | Current in the mas- ter transceiver | 35,27 mA | 31,67 mA |

Table 3-7: Calculation of a system with 15 BSM- slaves

1) Maximum Number of pre selected BSM-nodes (see calculation of pre-selected slaves)



3.7.4 Calculation of a system with 5 standard- and 10 BSM- slaves

| No. | Parameter | Condition V _{bat} = 18V | $R_{Master} = 900 \ \Omega$ | $R_{Master} = 1100 \ \Omega$ |
|-----|------------|---|-----------------------------|------------------------------|
| 1 | Step 3 + 4 | Standard Nodes = 5 R_Slave = 20 kΩ | 4,5 mA | 4,5 mA |
| | | BSM- Nodes = 10 I_ _{CS_1} = 1,24 mA | 12,4 mA | 12,4 mA |
| | I_R_Master | | 20 mA | 16,4 mA |
| | I_Bus_DOM | Current in the mas- ter transceiver | 36,9 mA | 33,3 mA |

| 2 | Step 5 + 6 | Standard Nodes = 5 R_Slave = 20 k Ω | 4,5 mA | 4,5 mA |
|---|------------|--|----------|----------|
| | | l _{_CS_1} = 1,24 mA BSM- nodes = 3 1) | 3,72 mA | 3,72 mA |
| | | I_ _{CS_2} = 3,85mA BSM- nodes = 3 1) | 11,55 mA | 11,55 mA |
| | I_R_Master | | 20 mA | 16,4 mA |
| | I_Bus_DOM | Current in the mas- ter transceiver | 39,77 mA | 35,77 mA |

Table 3-8: Calculation of a system with 5 standard and 10 BSM- slaves

1) Maximum Number of pre selected BSM-nodes (see calculation of pre-selected slaves)

| 1. | LIN Bus Shunt Slave Node Position Detection |
|----------------------------|--|
| in | Revision 1.0 December 10. 2008: Page 24 |
| LOCAL INTERCONNECT NETWORK | |

3.8 LIMITATIONS IN USE

The Bus Shunt Method has following constraints and is not fully LIN 2.1 compliant in the following aspects:

- During the configuration period the transceiver in the master must be capable to drive at least 40 mA at all allowed supply voltages for 9-T_{BIT} times – 4-T_{BIT} times after the falling edge of the break field.
- 2. Ground Shift Reduction. The used number of installed shunts in the system reduces the overall ground shift tolerance as well as V_{BAT} -Shift exceed the tolerances stated in the table below.

| Number of Shunts (1.25Ω max) | GND Shift tolerance [%V _{BAT}] | V_{BAT} Shift tolerance [%V _{BAT}] |
|------------------------------|--|--|
| 0 | 10 | 10 |
| 1 | 9.8 | 9.89 |
| 2 | 9.65 | 9.8 |
| 3 | 9.49 | 9.71 |
| 4 | 9.32 | 9.62 |
| 5 | 9.15 | 9.53 |
| 6 | 8.97 | 9.43 |
| 7 | 8.78 | 9.33 |
| 8 | 8.58 | 9.22 |
| 9 | 8.38 | 9.11 |
| 10 | 8.17 | 9.00 |
| 11 | 7.95 | 8.88 |
| 12 | 7.72 | 8.76 |
| 13 | 7.48 | 8.64 |
| 14 | 7.24 | 8.51 |
| 15 | 6.98 | 8.38 |

Table 3-9: Ground- and V_{BAT} shift Tolerances depending on the number of nodes